CLAIMS

What is claimed is:

1. A transcoder, comprising:

an input that receives a first signal having a first signal type from a first functional block;

a transcoder functional block that transforms the first signal having the first signal type thereby generating a second signal having a second signal type;

an output that transmits the second signal having the second signal type to a second functional block;

wherein the first signal type includes at least one a first modulation, a first code rate, a first symbol rate, and a first data rate; and

wherein the second signal type includes at least one a second modulation, a second code rate, a second symbol rate, and a second data rate.

2. The transcoder of claim 1, wherein:

the first signal type is a turbo coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

3. The transcoder of claim 1, wherein:

the first signal type is an LDPC (Low Density Parity Check) coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

4. The transcoder of claim 1, wherein:

the transcoder functional block is implemented within an integrated circuit.

5. The transcoder of claim 4, wherein:

the first functional block and the second functional block are functional blocks within the integrated circuit.

6. The transcoder of claim 4, wherein:

the first functional block is a satellite receiver that is operable to decode the first signal having the first signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

7. The transcoder of claim 4, wherein:

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operable to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operable to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

8. The transcoder of claim 7, wherein:

the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

9. The transcoder of claim 1, wherein:

the transcoder is implemented as at least one of a one to many transcoder, a uni-directional transcoder, and a bi-directional transcoder;

the one to many transcoder is operable to transform the first signal having the first signal type thereby generating the second signal having the second signal type and a third signal having the third signal type;

the uni-directional transcoder is operable to transform the first signal having the first signal type thereby generating the second signal having the second signal type when communicating in a first direction with respect to the transcoder;

the bi-directional transcoder is operable to transform the first signal having the first signal type thereby generating the second signal having the second signal type when information is communicated in a first direction with respect to the transcoder; and

the bi-directional transcoder is also operable to transform the fourth signal having the fourth signal type thereby generating the fifth signal having the fifth signal type when information is communicated in a second direction with respect to the transcoder.

10. The transcoder of claim 1, wherein:

the transcoder is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cable television system, and a cable modem communication system.

11. The transcoder of claim 1, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

12. The transcoder of claim 1, wherein:

a satellite signal, being a turbo coded signal and having an 8 PSK (Phase Shift Keying) modulation type, that is provided to a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner that is operable to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the first functional block is an 8 PSK (Phase Shift Keying) turbo code receiver;

the analog baseband signal is provided to the 8 PSK turbo code receiver that is operable to decode the analog baseband signal thereby generating a decoded baseband signal;

the analog baseband signal is the first signal having the first signal type that is provided to the transcoder functional block;

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that is operable to transform the first signal having the first signal type thereby generating the second signal having the second signal type;

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operable to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

13. The transcoder of claim 12, further comprising:

a microcontroller or a state machine that is operable to coordinate the communication and control of a Set Top Box (STB), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

14. The transcoder of claim 13, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

15. The transcoder of claim 14, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

16. A transcoder, comprising:

an input that receives a first signal from a first functional block;

wherein the first signal includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate.of approximately 41 Mbps (Mega-bits per second);

a transcoder functional block that transforms the first signal thereby generating a second signal;

an output that transmits the second signal to a second functional block; and

wherein the second signal includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

17. The transcoder of claim 16, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

18. The transcoder of claim 16, wherein:

the first functional block includes a the CMOS (Complementary Metal Oxide Semiconductor) satellite tuner;

the transcoder functional block includes an 8 PSK (8 Phase Shift Key) turbo code receiver and a DVB (Digital Video Broadcasting) encoder/modulator;

the second functional block includes a DAC (Digital to Analog Converter);

a satellite signal, being a turbo coded signal and having an 8 PSK modulation type, is provided to the CMOS satellite tuner that is operable to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the analog baseband signal is the first signal;

the analog baseband signal is provided from the CMOS satellite tuner to the 8 PSK turbo code receiver that is operable to decode the analog baseband signal thereby generating a decoded baseband signal;

the DVB encoder/modulator receives the decoded baseband signal and generates a digital DVB signal;

the digital DVB signal is the second signal;

the DAC (Digital to Analog Converter) is operable to transform the second signal from a digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operable to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

19. The transcoder of claim 18, further comprising:

a microcontroller or a state machine that is operable to coordinate the communication and control of a STB (Set Top Box), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

20. The transcoder of claim 19, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

21. The transcoder of claim 20, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

22. The transcoder of claim 16, wherein:

the first signal is a turbo coded signal.

23. A transcoder, comprising:

an input that receives a first signal from a first functional block;

wherein the first signal includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second);

a transcoder functional block that transforms the first signal thereby generating a second signal;

an output that transmits the second signal to a second functional block; and

wherein the second signal includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

24. The transcoder of claim 23, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

25. The transcoder of claim 23, wherein:

the first functional block includes a the CMOS (Complementary Metal Oxide Semiconductor) satellite tuner;

the transcoder functional block includes an 8 PSK (8 Phase Shift Key) LDPC (Low Density Parity Check) code receiver and a DVB (Digital Video Broadcasting) encoder/modulator;

the second functional block includes a DAC (Digital to Analog Converter);

a satellite signal, being an LDPC coded signal and having an 8 PSK modulation type, is provided to the CMOS satellite tuner that is operable to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the analog baseband signal is the first signal;

the analog baseband signal is provided from the CMOS satellite tuner to the 8 PSK LDPC code receiver that is operable to decode the analog baseband signal thereby generating a decoded baseband signal;

the DVB encoder/modulator receives the decoded baseband signal and generates a digital DVB signal;

the digital DVB signal is the second signal;

the DAC (Digital to Analog Converter) is operable to transform the second signal from a digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operable to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

26. The transcoder of claim 25, further comprising:

a microcontroller or a state machine that is operable to coordinate the communication and control of a STB (Set Top Box), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

27. The transcoder of claim 26, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

28. The transcoder of claim 27, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

29. The transcoder of claim 23, wherein:

the first signal is an LDPC coded signal.

30. An integrated circuit, comprising:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner that receives a satellite signal, the satellite signal being a turbo coded signal and having an 8 PSK (Phase Shift Keying) modulation type;

wherein the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

an 8 PSK turbo code receiver that receives the analog baseband signal;

wherein the 8 PSK turbo code receiver is operable to decode the analog baseband signal thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal;

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal;

a DAC (Digital to Analog Converter) that is operable to transform the digital DVB signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operable to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

31. The integrated circuit of claim 30, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK turbo code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

32. The integrated circuit of claim 30, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

33. The integrated circuit of claim 32, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

34. The integrated circuit of claim 33, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

35. An integrated circuit, comprising:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner that receives a satellite signal, the satellite signal being an LDPC (Low Density Parity Check) coded signal and having an 8 PSK (Phase Shift Keying) modulation type;

wherein the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

an 8 PSK LDPC code receiver that receives the analog baseband signal;

wherein the 8 PSK LDPC code receiver is operable to decode the analog baseband signal thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal;

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal;

a DAC (Digital to Analog Converter) that is operable to transform the digital DVB signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operable to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

36. The integrated circuit of claim 35, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK LDPC code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

37. The integrated circuit of claim 35, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

38. The integrated circuit of claim 37, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

39. The integrated circuit of claim 38, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

40. An integrated circuit, comprising:

an 8 PSK (Phase Shift Key) turbo code receiver that receives the analog baseband signal;

wherein the 8 PSK turbo code receiver is operable to decode an analog baseband signal having I, Q (In-phase, Quadrature) components thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal;

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal; and

a DAC (Digital to Analog Converter) that is operable to transform the digital DVB signal into an analog IF (Intermediate Frequency) signal.

41. The integrated circuit of claim 40, wherein:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner, communicatively coupled to the integrated circuit, receives a satellite signal, the satellite signal being a turbo coded signal and having an 8 PSK modulation type; and

the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate the analog baseband signal having I, Q components.

42. The integrated circuit of claim 40, wherein:

an up-converter functional block, communicatively coupled to the integrated circuit, up-converts the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

43. The integrated circuit of claim 40, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK turbo code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

44. The integrated circuit of claim 40, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

45. The integrated circuit of claim 44, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

46. The integrated circuit of claim 45, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

47. An integrated circuit, comprising:

an 8 PSK (Phase Shift Key) LDPC (Low Density Parity Check) code receiver that receives the analog baseband signal;

wherein the 8 PSK LDPC code receiver is operable to decode an analog baseband signal having I, Q (In-phase, Quadrature) components thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal;

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal; and

a DAC (Digital to Analog Converter) that is operable to transform the digital DVB signal into an analog IF (Intermediate Frequency) signal.

48. The integrated circuit of claim 47, wherein:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner, communicatively coupled to the integrated circuit, receives a satellite signal, the satellite signal being an LDPC coded signal and having an 8 PSK modulation type; and

the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate the analog baseband signal having I, Q components.

49. The integrated circuit of claim 47, wherein:

an up-converter functional block, communicatively coupled to the integrated circuit, up-converts the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

50. The integrated circuit of claim 47, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK LDPC code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

51. The integrated circuit of claim 47, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

52. The integrated circuit of claim 51, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

53. The integrated circuit of claim 52, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

54. An integrated circuit, comprising:

an 8 PSK (Phase Shift Key) turbo code receiver that receives the analog baseband signal;

wherein the 8 PSK turbo code receiver is operable to decode an analog baseband signal having I, Q (In-phase, Quadrature) components thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal; and

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal.

55. The integrated circuit of claim 54, wherein:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner, communicatively coupled to the integrated circuit, receives a satellite signal, the satellite signal being a turbo coded signal and having an 8 PSK modulation type; and

the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate the analog baseband signal having I, Q components.

56. The integrated circuit of claim 54, wherein:

a DAC (Digital to Analog Converter), communicatively coupled to the integrated circuit, transforms the digital DVB signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block, communicatively coupled to the DAC, up-converts the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

57. The integrated circuit of claim 54, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK turbo code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

58. The integrated circuit of claim 54, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

59. The integrated circuit of claim 58, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

60. The integrated circuit of claim 59, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

61. An integrated circuit, comprising:

an 8 PSK (Phase Shift Key) LDPC (Low Density Parity Check) code receiver that receives the analog baseband signal;

wherein the 8 PSK LDPC code receiver is operable to decode an analog baseband signal having I, Q (In-phase, Quadrature) components thereby generating a decoded baseband signal;

a DVB (Digital Video Broadcasting) encoder/modulator that receives the decoded baseband signal; and

wherein the DVB encoder/modulator is operable to transform the decoded baseband signal thereby generating a digital DVB signal.

62. The integrated circuit of claim 61, wherein:

a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner, communicatively coupled to the integrated circuit, receives a satellite signal, the satellite signal being an LDPC coded signal and having an 8 PSK modulation type; and

the CMOS satellite tuner is operable to perform tuning and down-converting of the satellite signal to generate the analog baseband signal having I, Q components.

63. The integrated circuit of claim 61, wherein:

a DAC (Digital to Analog Converter), communicatively coupled to the integrated circuit, transforms the digital DVB signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block, communicatively coupled to the DAC, up-converts the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

64. The integrated circuit of claim 61, further comprising a MPEG-2 (Motion Picture Expert Group, level 2) transport processor interposed between the 8 PSK LDPC code receiver and the DVB encoder/modulator;

wherein the MPEG-2 transport processor includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the decoded baseband signal;

the PCR time stamp correction functional block is operable to keep a time base of the decoded baseband signal constant; and

the null packet insertion functional block is operable to insert null packets into the decoded baseband signal thereby ensuring a constant data rate of the decoded baseband signal.

65. The integrated circuit of claim 61, wherein:

a microcontroller or a state machine, communicatively coupled to the integrated circuit, is operable to coordinate the communication and control of a STB (Set Top Box), to which the integrated circuit is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the integrated circuit is also communicatively coupled.

66. The integrated circuit of claim 65, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

67. The integrated circuit of claim 66, wherein each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

68. A transcoding processing method, the method comprising:

receiving a first signal having a first signal type from a first functional block;

transcoding the first signal having the first signal type thereby generating a second signal having a second signal type;

outputting the second signal having the second signal type to a second functional block;

wherein the first signal type includes at least one a first modulation, a first code rate, a first symbol rate, and a first data rate; and

wherein the second signal type includes at least one a second modulation, a second code rate, a second symbol rate, and a second data rate.

69. The method of claim 68, wherein:

the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

70. The method of claim 69, wherein:

the first signal is a turbo coded signal.

71. The method of claim 68, wherein:

the first signal type is an LDPC (Low Density Parity Check) coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

72. The method of claim 71, wherein:

the first signal is a turbo coded signal.

73. The method of claim 68, wherein:

the first functional block includes a satellite receiver that is operable to decode the first signal having the first signal type; and

the second functional block includes a modulator and a Digital to Analog Converter (DAC) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

74. The method of claim 68, wherein:

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operable to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operable to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

75. The method of claim 74, wherein:

the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

76. A transcoding processing method, the method comprising:

receiving a first signal having a first signal type from a first functional block;

wherein the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second)

transcoding the first signal having the first signal type thereby generating a second signal having a second signal type;

wherein the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps;

outputting the second signal having the second signal type to a second functional block; and

wherein the first signal is a turbo coded signal.

77. The method of claim 76, wherein:

the first functional block includes a satellite receiver that is operable to decode the first signal having the first signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

78. The method of claim 76, wherein:

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operable to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operable to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

79. The method of claim 78, wherein the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

80. A transcoding processing method, the method comprising:

receiving a first signal having a first signal type from a first functional block;

wherein the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second)

transcoding the first signal having the first signal type thereby generating a second signal having a second signal type;

wherein the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30. 5 Mbps;

outputting the second signal having the second signal type to a second functional block; and

wherein the first signal is an LDPC (Low Density Parity Check) coded signal.

81. The method of claim 80, wherein:

the first functional block includes a satellite receiver that is operable to decode the first signal having the first signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

82. The method of claim 80, wherein:

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operable to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operable to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operable to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes a modulator and a DAC (Digital to Analog Converter) that is operable to transform the second signal having the second signal type from a digital signal into an analog signal.

83. The method of claim 82, wherein the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.